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# Military/Civilian Mixed-Mode Global Positioning System (GPS) Receiver (MMGR)

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**Abstract**—This paper describes plans and progress made on the MMGR program funded jointly by Air Force Research Laboratory (AFRL), GPS Joint Program Office (JPO) and industry that started in April 2003.

The AFRL Dual Use Science and Technology (DUS&T) MMGR objective of meeting pervasive defense system requirements and civilian needs for ultra-small GPS receiver technology is dependent in part upon the creation of multi-L-band reconfigurable receiver integrated circuitry that supports Coarse Acquisition (C/A), Precision Encrypted [P(Y)], and Military (M)-code operation. The creation of this military/civilian circuitry with reduced cost and improved speed-power-weight capabilities is enabled through adaptation of commercial and radiation tolerant design and manufacturing abilities that leverage synergies across proven, legacy GPS receiver architectures. The Honeywell contribution to the program includes demonstration of the feasibility of applying bulk or silicon on insulator (SOI) 1.8V Complementary Metal Oxide Semiconductor (CMOS) technology to create a working radio frequency (RF) analog front end for miniature GPS receivers. This shows a path to a single chip GPS receiver via combined RF analog and advanced sub-micron ultra large scale integrated digital circuits.

The Honeywell/Rockwell Collins MMGR program will start with a minimum configuration of the GPS receiver (e.g. low end commercial GPS) and develop a new RF front-end design using mixed mode CMOS technology with lowest cost components and processes over the first year of the program. The front-end Application Specific Integrated Circuit (ASIC) design will have a modular and flexible architecture based on reusable macro-cells. This initial RF front-end design will be evolved and targeted to meet specific commercial, military and space application requirements during the subsequent development iterations over the last two years of the program and beyond.

Rockwell Collins will demonstrate feasibility of using a digital device to create an M-code capable, high anti-jam GPS system. This shows a path to an adaptable MMGR that enables flexibility and easy upgradeability for both military and commercial GPS receivers and adheres to GPS Modernization/GPS III receiver specifications. The emphasis of the Rockwell Collins task is to improve anti-jam (AJ) and anti-interference capability of the GPS receivers through miniaturization of the anti-jamming (AJ) electronics and improvements in ultra-tight coupling (UTC) of a GPS receiver and an Inertial Measurement Unit (IMU).

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## 1. INTRODUCTION

Commercial industry is attempting to create miniature GPS technology; however, the mixture of analog and digital circuitry on a single integrated circuit has proven difficult. The existing solutions consist of several components and address single band, simple civilian GPS systems [1,2]. This manufacturing challenge can be overcome by separating the analog technology and limited digital functionality within a mixed mode front end ASIC while relegating the digital technology (back end) within the receiver. A very flexible architecture and high anti-jamming and anti-interference capability as well as potential for small size and low power of proposed approach differentiate it from existing solutions. The requirements for anti-jamming or interference become equally ubiquitous in the military as in commercial applications as the radio wave bands saturate by wireless communications. Frequently unintentional

interference is also generated by other electronics collocated with GPS receiver. Some of the proposed solutions to interference may be also applied to loss of GPS signal caused by physical features of environment like tall buildings, mountains, forest and walls. As GPS becomes more robust and its availability increases it will be used more often in highly reliable systems and applications. Therefore our GPS architecture may also help in broadening applicability of GPS. In this paper we describe how the modular architecture of back end could allow for making GPS receivers with legacy and modernized encryption functions. The modular architecture of front end will lead to many versions of the front end ASIC that would be compatible with one or all GPS frequencies: L2, L5, L1 and with different filtering and dynamic range environment e.g. intentional jamming on the battle field versus weak signal environment. When completed this technology might be applied to commercial applications such as Federal Communications Commission (FCC) enhanced 911 for cell phones, lost children locators, vehicle alarm systems, shipper tracking service, personal wallet imbedded GPS receiver, etc. The military applications include precision munitions, reentry vehicles, Military Space Plane, Space Based Radar, Space Based Laser, Common Aero Vehicle, GPS upgrades, autonomous satellites, personal GPS, unmanned aerial vehicles, etc.

## 2. ARCHITECTURE OF FRONT END

The MMGR front end development at Honeywell will start with a minimum configuration of the GPS receiver (e.g. low-end commercial GPS) and define a set of requirements for the RF front-end. We will flow down these requirements into the main macro-cells of an ASIC to facilitate modular and flexible architecture for the RF front-end. The initial RF front-end design will be updated and enhanced to meet the commercial, military and possibly space application requirements during the subsequent development iterations over the remainder of the program. The basic technology variations to be incorporated in the mixed-mode, multi-user GPS front-end are listed in Table 1.

Each function can be implemented in the wide range of performance from the hand-held to military receiver. These technologies become the building blocks of the GPS receiver front end as shown in Figure 1.

**Table 1. Honeywell's dual use macro cell approach for commercial and military applications.**

Function	Minimum-cost commercial GPS receiver	Maximum performance military GPS receiver
Architecture	Dual Heterodyne to low intermediate frequency (IF) integrated active filters for minimum system cost	Single conversion Receiver (Rx) optimized for high Spurious Free Dynamic Range (SFDR)
Preselection filter	L1, Surface Acoustic Wave (SAW) / miniature thin film resonators	Miniature thin film resonators for L1, L2 and future L5
Low noise amplifier	Low current on-chip amplifiers with sub 1dB noise figure	Adjustable gain/intercept point amplifiers for optimum SFDR
Local Oscillator	L1 low phase noise optimized frequency synthesizer.	Enhanced for multi-band operation.
A/D converter for IF signal sampling	Integrated 2-bit flash Analog to Digital (A/D) converter minimizes power consumption	10-bit pipelined A/D converter enhances ranging precision. Separate ASIC

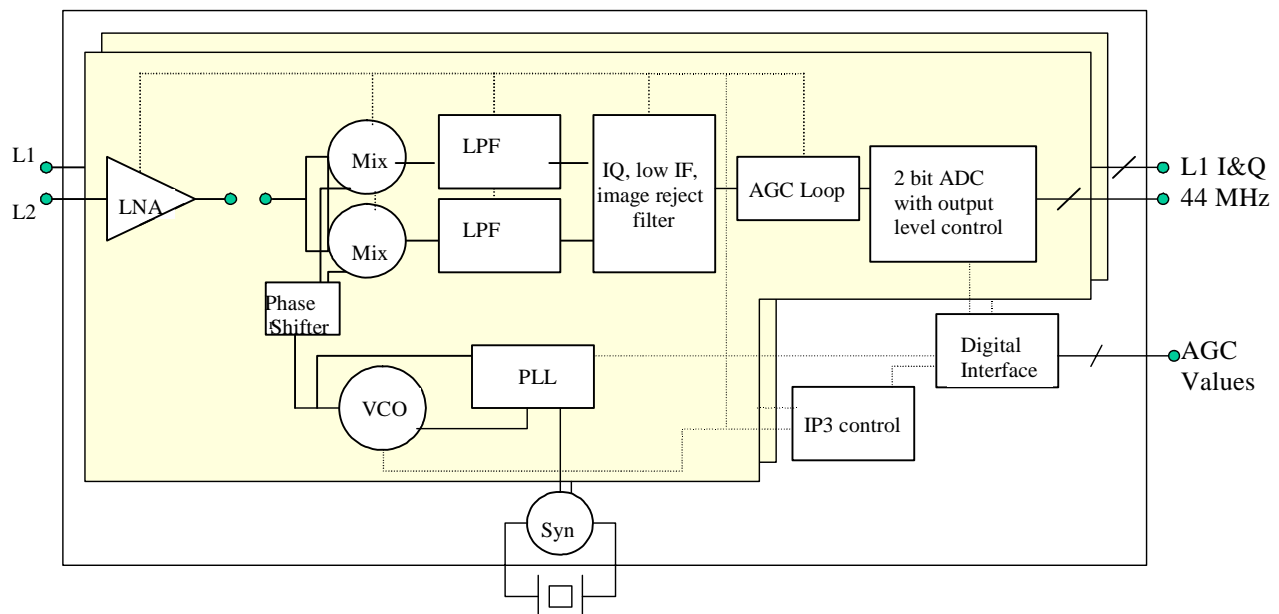


Figure 1. Flexible Honeywell GPS front end ASIC architecture for two or more (e.g. L5) frequency channels can be extended from handheld commercial to military applications (LPF - Low Pass Filter, AGC - Automatic Gain Control, ADC - Analog to Digital Converter, IP3 - 3rd order Intercept Point, VCO - Voltage Controlled Oscillator, Mix - Mixer, PLL - Phase Locked Loop, LNA-low noise amplifier, Syn-synthesizer).

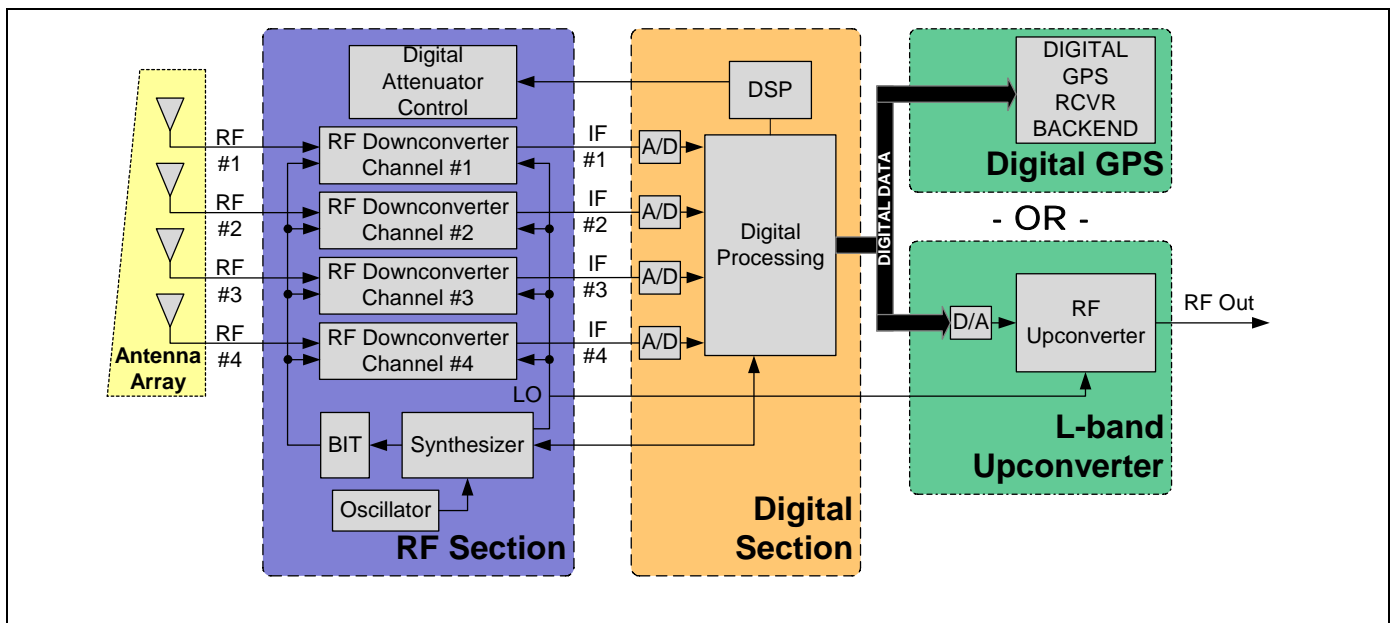


Figure 2. MIDAS Digital AJ Architecture block diagram

### 3. DUAL USE AJ ARCHITECTURE

Rockwell Collins recognizes that both commercial and military GPS users have needs for reducing the signals that interfere with GPS navigation. These interferers may consist of television transmitter harmonics, multipath due to

reflected GPS satellite signals, as well as intentional jamming encountered on a battlefield. Rockwell Collins' competencies in AJ systems and UTC GPS/IMU systems provide solutions that overlap the commercial and military markets.

## AJ Systems

AJ systems, such as Rockwell Collins' Miniature Integrated Digital Anti-jam System (MIDAS), provide additional AJ protection for military GPS users. Figure 2 shows the overall block diagram for the four-element MIDAS AJ system that will be used as the starting point for the MMGR Digital AJ ASIC. The antenna array receives the RF signals using four separate antenna elements. From there, the signals flow into the RF section that downconverts them to an intermediate frequency sufficient for processing by the digital section. An analog-to-digital converter transforms the signals into the digital domain. The combination of a Digital Signal Processor (DSP) processor and hardware circuitry conditions the data, calculates the weights and combines the four filtered signals to optimally reduce the received jamming signal. This single digital signal representation then flows to the output stage. Here the signal can either connect to a Rockwell Collins NavStrike™-digital receiver or be converted to analog and upconverted back to L-band. This allows use of either newer digital input receivers or legacy RF input receivers as called for by the user's needs.

While targeted predominantly for military users, AJ systems can also be used in a commercial environment to attenuate other interfering signals. Current AJ systems add onto the basic GPS receiver. Thus, minimizing size, weight and power (SWAP) becomes critically important. MIDAS implements the digital processing section using a field programmable gate array (FPGA). FPGAs offer maximum flexibility of design. However they use a great deal of power and take up significant amounts of circuit card real estate. This makes the digital section a clear target for integration into an ASIC which will be addressed by Rockwell Collins as part of the MMGR program.

## AJ ASIC Requirements

Table 2 captures the main requirements levied on the AJ ASIC. To the maximum extent possible, the ASIC requirements will meet or exceed these goals, though tradeoffs may be required to balance performance versus cost and SWAP. Though ASICs inherently possess less flexibility than FPGAs, this ASIC will be designed with flexibility in mind as the number of possible AJ applications is constantly on the increase. Rockwell Collins anticipates that future navigation systems will consist of an integrated AJ unit and GPS receiver in the same package. This ASIC provides a significant step in that direction and this future need will be considered as the design progresses.

Table 2. MMGR Digital AJ ASIC Performance Goals Target Military and Commercial Needs

REQUIREMENT	GOAL
<b>Codes</b>	<b>C/A, P(Y), M</b>
<b>Antenna Elements/Channels</b>	<b>7</b>
<b>Beamforming Outputs</b>	<b>16</b>
<b>AJ Improvement</b>	<b>Greater than 30 dB</b>
<b>Cost</b>	<b>Suitable for high volume production</b>
<b>Targeted Platforms</b>	<b>Airborne</b>
<b>Commercial</b>	<b>Airborne, Munitions, Handhelds</b>
<b>Military</b>	<b>Airborne, Munitions, Handhelds</b>

## UTC

For systems that include an IMU, such as many aircraft, UTC can provide additional AJ/interference rejection with no additional hardware. Figure 3 shows the basic operation of a UTC system. The Navigator uses the measurements from the IMU to drive the GPS tracking loops. The Navigator then blends the IMU measurements with the GPS measurements to produce its navigation solution. As in the case of the AJ systems, the UTC work to date has concentrated on military applications that use P(Y) code. Commercial applications use C/A code exclusively. Thus, the military-centric UTC algorithms require modifications to work with C/A code.

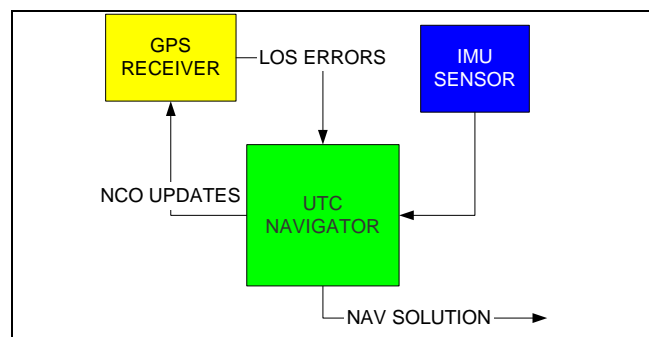


Figure 3. UTC Increases GPS AJ (LOS-line of sight, NCO-numerically controlled oscillator).

## M-code Compatibility

The GPS JPO has several efforts currently underway that will place a new M-code into service during the next few years. Thus, M-code compatibility is a goal for the MMGR program. The JPO's current Modernized User Equipment (MUE) program addresses the major impact that M-code will have on the architecture and design of military GPS receivers. Rockwell Collins will explore the M-code impacts to both AJ systems and UTC as part of the MMGR program.

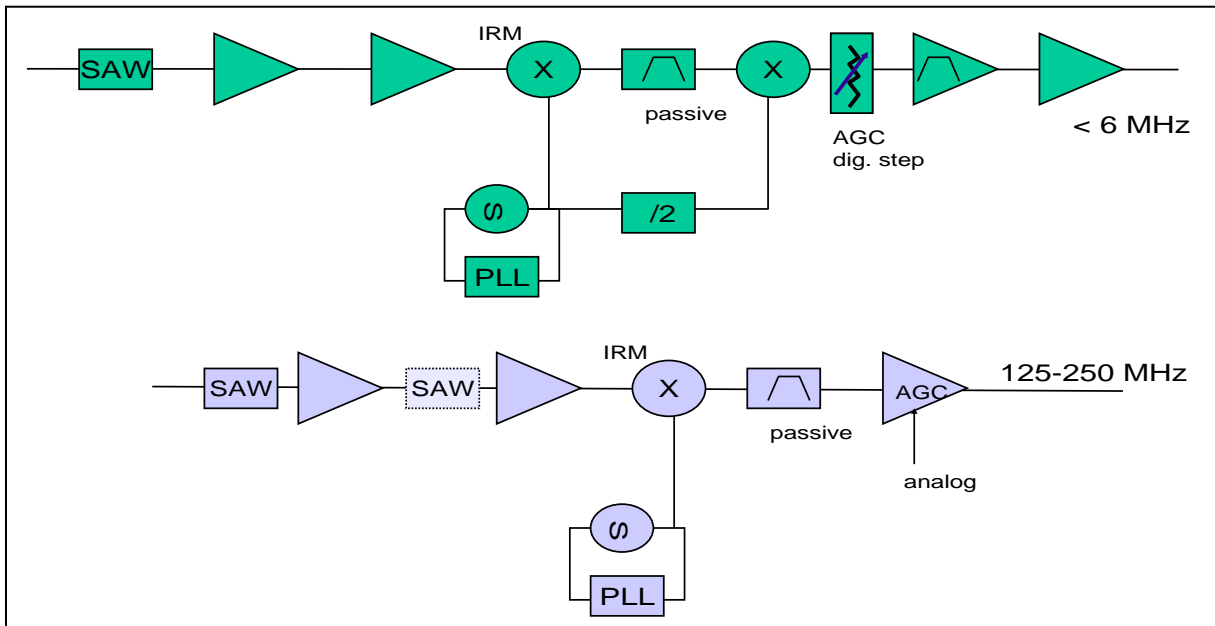


Figure 4. Architecture of the Commercial (top) and Military (bottom) GPS Receiver Front End

For the AJ ASIC, M-code compatibility will be included as a design requirement. M-code's higher bandwidth will require a higher sampling rate compared to the existing P(Y) code system. For M-code compatibility with UTC, the existing UTC algorithms will be modified to operate with the new M-code signal as well as C/A- and P-codes.

#### 4. BUILDING BLOCKS OF FRONT END

The differences between commercial and military receiver architectures are shown in Figure 4. While the commercial and military receivers have different frequency plans, we defined a list of common macrocells that will become building blocks. Functionality of the macrocells will be always the same even though the frequency and other parameters may vary. The macrocells include: three different gain low noise amplifiers (LNA), Mixer, IF (Intermediate Frequency) Filter, Low IF Mixer, Baseband Filter, Baseband amplifier, and the Analog to Digital Converter.

Key performance specifications of the parts are driven by the desire to work from a single 1.8V power supply allowing future integration with fine geometry CMOS or SOI CMOS ASIC technologies. Our early work indicates that this advanced ASIC technology provides less than 2 dB noise figures and system gains tailorable from 60 to 100dB. Key areas for concentrating our efforts is providing the ability to work at the L1, L2 and L5 frequency bands with minimal configuration changes and distributing gain and compression points through out the system in such a fashion

as to preserve both commercial and military IP3 (3<sup>rd</sup> harmonic intercept) requirements.

#### 5. DUAL USE AJ BUILDING BLOCKS

##### AJ ASIC

Rockwell Collins currently is gathering the detailed requirements for the ASIC based on industry needs and performance goals shown above in Table 2. A number of trade studies are currently underway to transform the performance goals into actual ASIC requirements. The trades currently being performed include studies into:

- Number of antenna elements versus ASIC pin count and package size
- Number of beam outputs vs. pin count
- M-code sampling rate vs. P-code rate
- Memory requirements
  - On-chip vs. off-chip
- Number of required multipliers
  - Overall chip size
  - Capabilities for STAP and SFAP
- Chainable vs. self-contained ASIC

The preliminary design for the chip to be developed under MMGR is shown in Figure 5. Following solidification of the requirements and overall system design, development of the actual ASIC design will begin. The design will first target FPGAs so that proper operation can be verified before committing it to silicon. Once the design has been verified on the FPGAs, the actual ASIC can be fabricated. The ASIC will then be tested within the AJ system in place of the FPGAs to verify that it performs as desired.

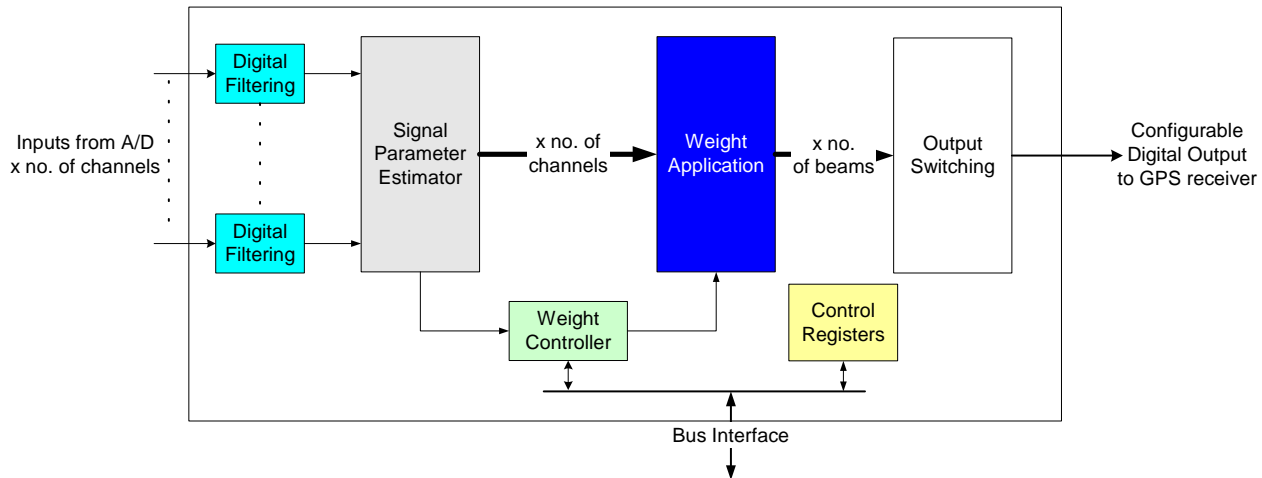


Figure 5. M-code Digital AJ ASIC Block Diagram (x describes adjustable number of channels/beams in the architecture)

### M- and C/A-code UTC

Rockwell Collins development of UTC algorithms for M- and C/A-codes, referred to as UTC-MCA, will build off of our P(Y)-code algorithms. These algorithms have been verified using our Rockwell Collins' Tracking Simulator (RCTS) program. RCTS uses Matlab to simulate the operation of a GPS receiver system. It allows the engineers to vary a large number of tracking loop and environmental variables to simulate real-world situations encountered by GPS receivers. RCTS currently contains the Rockwell Collins' P(Y)-code UTC algorithm. Under MMGR, this software will be extended first to add C/A-code capability and then to add M-code. Following addition of these new capabilities, UTC-MCA will be run against a suite of jamming scenarios to quantify the AJ improvement that is possible with these improved algorithms.

## 6. CONCLUSIONS

Honeywell and Rockwell Collins have developed a unique architecture for GPS receiver that could be used in many civilian and military applications and feature small size and low power. The antijamming and anti-interference capability is emphasized because of pervasive needs in this area. Our approach has been partially validated by designing and fabricating set of RF front end macrocells that should meet the broad set of requirements. Simultaneously we have validated the antijamming ASIC architecture and ultra tight coupled GPS and IMU through simulations. First hardware validation of architecture components is expected in 2004 and the final GPS receiver demo is planned for early 2006.

We envision a common architecture for military and commercial receivers enables maximum system synergy for both the supplier and customer over commercial and military, avionics, aerospace and land based applications.

## REFERENCES

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